Remarks

Applicants respectfully request reconsideration of the present application in view of the foregoing amendments and the following remarks. Claims 1-13 remain pending. In response to a previously issued restriction requirement, claims 1-13 were elected and claims 14-65 are withdrawn. Claim 1 is independent. No claims have been allowed. Claim 1 has been amended for reasons of clarity.

Patentability of Claims 1-13 over Fung in view of Wallace under 35 U.S.C. § 103(a)

Claims 1-13 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent Publication No. 2005/0204325 to Fung et al. ("Fung") in view of U.S. Patent Publication No. 2006/0117280 to Wallace ("Wallace"). These rejections are respectfully traversed.

Claim 1

Independent claim 1 is directed to a method that recites in part: "identifying the at least one memory module having the undesirable timing delay" and "selectively re-implementing the at least one memory module having the undesirable timing delay using the second set of logic blocks in the event that re-implementation using the second set of logic blocks reduces the undesirable timing delay of the at least one memory module having the undesirable timing delay" (emphasis added).

Fung is understood to describe a method for mapping logic design memory into physical memory devices of a programmable logic device. The Action directs attention to several different sections in Fung but Applicants respectfully submit that none of those sections, nor any other section of Fung, are understood to teach or suggest identifying the at least one memory

module having the undesirable timing delay, let alone selectively re-implementing the at least one memory module having the undesirable timing delay using the second set of logic blocks in the event that re-implementation using the second set of logic blocks reduces the undesirable timing delay of the at least one memory module having the undesirable timing delay, as recited in independent claim 1.

For example, Fung states in para. [0040] that "the logic design to hardware implements the logic design memory in physical memory devices by "slicing" the logic design memory into smaller pieces and distributing the resultant "memory slices" to particular physical memory devices at particular locations on the programmable logic device." Applicants respectfully submit, however, that "slicing" logic design memory into smaller pieces and distributing them does not teach or suggest identifying the at least one memory module having the undesirable timing delay, as recited in independent claim 1. Additionally, and because Fung does not teach or suggest this limitation, Applicants respectfully submit that Fung also does not teach or suggest selectively re-implementing the at least one memory module having the undesirable timing delay using the second set of logic blocks in the event that re-implementation using the second set of logic blocks reduces the undesirable timing delay of the at least one memory module having the undesirable timing delay, as recited in independent claim 1.

Furthermore, Fung does not teach or suggest at least a first logic block of the said second set having a pin that is logically equivalent to said at least one critical pin of the at least one logic block of said first set, as noted in the Action at page 5.

Applicants respectfully submit that Wallace does not cure the deficiencies of Fung. Wallace is understood to describe input equivalence within a digital logic circuit. For example, paragraphs [0028] to [0036] describe three types of input equivalence (single gate and single pin;

multi-gate and single pin; and multi-pin). Wallace also describes optimization opportunities offered by exploitation of such equivalencies (*see, e.g.*, para. [0037]). Applicants respectfully submit, however, that Wallace does not teach or suggest a critical pin, let alone a first logic block of the said second set having a pin that is logically equivalent to said at least one critical pin of the at least one logic block of said first set, as recited in independent claim 1.

Furthermore, nothing in Wallace is understood to teach or suggest identifying the at least one memory module having the undesirable timing delay, let alone selectively re-implementing the at least one memory module having the undesirable timing delay using the second set of logic blocks in the event that re-implementation using the second set of logic blocks reduces the undesirable timing delay of the at least one memory module having the undesirable timing delay, as recited in independent claim 1.

Therefore, Applicants respectfully submit that Fung and Wallace, individually or in combination, do not teach or suggest the limitations of independent claim 1. Accordingly, Applicants respectfully submit that the 35 U.S.C. § 103(a) rejection of independent claim 1 should be withdrawn and such action is respectfully requested.

Claims 2-13

Dependent claims 2-13 depend directly or indirectly from independent claim 1 and are allowable for at least the reasons recited above with respect to their parent claim 1.

Moreover, claims 2-13 recite combinations of features that are independently patentable. For example, Applicants respectfully submit that Fung and Wallace, either individually or in combination, do not teach or suggest a method "wherein the act of identifying the at least one memory module comprises performing physical timing analysis on at least said one memory

module, the method further comprising performing physical timing analysis on said at least one memory module to identify the at least one critical pin of said first set of at least one logic block, and wherein the method further comprises performing physical timing analysis on the re-implemented memory module using the second set of logic blocks prior to selecting the re-implementation of the at least one memory module using the second set of logic blocks," as recited in dependent claim 6.

As another example, Applicants respectfully submit that Fung and Wallace, either individually or in combination, do not teach or suggest a method "comprising the act of reversing the re-implementation to an implementation of the at least one memory module using the first set of logic blocks in the event the undesirable timing delay of the at least one memory module is not sufficiently reduced upon re-implementation using the second set of logic blocks," as recited in dependent claim 7.

Accordingly, Applicants respectfully submit that the 35 U.S.C. § 103(a) rejections of dependent claims 2-13 should be withdrawn and such action is respectfully requested.

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Application Number 10/785,608

Request for Interview

If any issues remain, the Examiner is formally requested to contact the undersigned attorney prior to issuance of the next Office Action in order to arrange a telephonic interview. It is believed that a brief discussion of the merits of the present application may expedite prosecution. Applicants submit the foregoing Response so that the Examiner may fully evaluate Applicants' position, thereby enabling the interview to be more focused.

This request is being made under MPEP § 713.01, which indicates that an interview may be arranged in advance by a written request.

Conclusion

The claims in their present form should now be allowable. Such action is respectfully requested.

Respectfully submitted,

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